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Design and Implementation of Optimized LDPC for SDR Applications

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Abstract

LDPC is a promising error correction protocol, which is widely useful for low-end wireless protocol standards. This lightweight protocol mechanism is suitable for basic SDR applications. The same is not true for high-end wireless communication due to its limitations. Since technological scaling on its own is insufficient to satisfy today's SDR architectures with these wireless standards. Hence by reducing the decoding complexity and by increasing capacity performance. We use this Low-Density Parity-Check codes in SDR based wireless communication platform. The major limitation of conventional LDPC code is high latency and power consumption with top design complexity. To overcome such a problem, the optimized LDPC encoding and decoding are proposed with less lag and power consumption without degrading the performance of the conventional design. The proposed model offers less hardware complexity used in telecommunication applications. This methodology is implemented and synthesized using Xilinx ISE tool.

Disciplinary: Electronics and Communication Engineering.

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1. Introduction

Software-defined radio (SDR) is used in several domains but primarily in the communication market. Major applications of this technology are Mobile communication, Local area wireless networks, Personal area networks and Remote broadcasting. We refer to applications where it is beneficial to have the ability to modify a modulation and encoding scheme. SDRs also outperform conventional hardware-only radios in these respects, due to their quick adaption of operations as per the environment requirement on the fly through software. The technological advancement in

the field of high-speed analog to digital converters (ADCs) and high-end Field Programmable Gate Arrays (FPGAs) have attracted research over SDRs in recent days. The SDR is a complicated tool that performs many complex tasks simultaneously to enable the smooth transmission and reception of data over the communication field. An interdependent sequence of operations that collect information in the transmitter end is usually part of a digital communication network.

It is sent to the receiver as prior information for processing and decoding without error. The reconstituted version of the original information signal may be speech, music or video. The error between the reconstituted or decoded signal and the original signal should be very small in all senses. Methods like quantization are utilized to interpret the information signal in binary form. This encoding/ decoding concept is vital in all forms of error-free digital communication platforms. The proposed method describes one such method in the SDR domain. This methodology proves to be the power-optimized algorithm, which is the main constraints of the applications evolved over SDR architectures.

The transmitter digitally processes the information in binary code, which is then converted into an electromagnetic sinusoidal waveform. Its physical characteristics include signal amplitude, carrier frequency and phase. On the other end of the communication scenario, receiver evaluates accurately the features of the intercepted modulated waveform, which transmitted through a potentially twisted and distortion-filled medium. The input of the transmitter and the output of the receiver derives a digital source and digital sink. Figure 1 shows the source and destination of the digital communication network's basic building blocks.

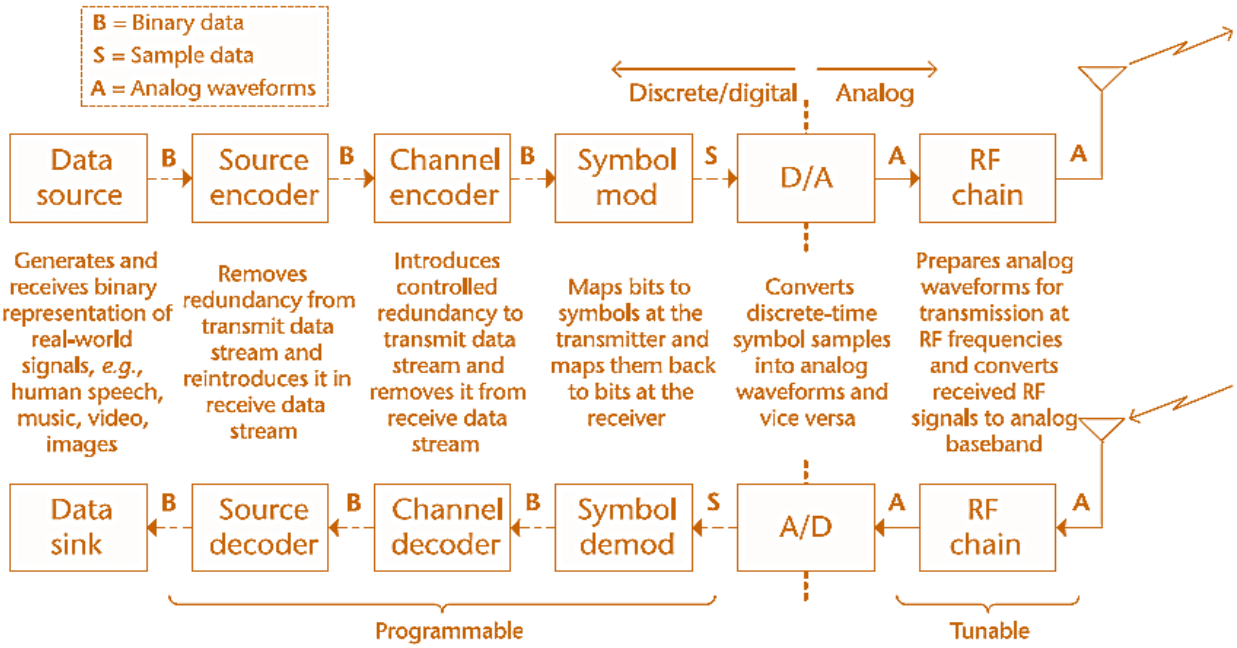

Figure 1: SDR general block diagram

The conversion of the source data into binary data then to symbol and vice versa is the complicated phases of the digital communication process. The same is taken care of by the processing elements mostly by DSP algorithms or by using the processing elements of reconfigurable FPGAs. The proposed power efficient algorithm is executed here in Xilinx platform.

When binary information is introduced into the sender, the first function is to delete all redundant/repeated binary patterns from the data so that transmission capacity is enhanced. This is done with the root block encoder that is programmed to remove all redundancy information. The source decoder reintroduces redundancy in the receiver to restore the binary information in its original form when the redundancy is removed from the binary data of the transmitter. To protect the information stream from possible errors that are introduced over a noisy channel during the transmission process, a channels encoder is used to add a fixed amount of redundant data.

A channel decoder eliminates this controlled redundancy, and binary information is returned to its original form. The next step is to convert binary data into specific electromagnetic waveform properties such as amplitude, frequency and phase. This is achieved using a modulation projection method. The receiver also transforms the electromagnetic waveform into a binary picture from the demodulation process. The discrete block samples are eventually re-sampled and turned into an analog waveform baseband with a digital to analog converter before being passed on to the RF frequency through the front-end communications network radio frequencies. The reverse is performed on the receiver when, before sampling and processing by an analog-to-digital converter, the intercepted analog signal is transformed by RFFE to the baseband frequency.

Low-density parity codes have shown a significant error beyond the Shannon limit in the output correction. Reasonable correction efficiency ensures secure and efficient communication. But the LDPC decoding algorithm must run effectively to satisfy the cost, time, power, and bandwidth requirements of the target applications. The generated codes should also meet the output error rate criteria for these applications. Much research work has been carried out on the design development and implementation of this LDPC code since its rediscovery. The LDPC codes can be designed in a full room using parameters like diameter, rate and length. The target focus of this research is to fix the standard framework to produce efficient LDPC codes. Developing the system with better performances, error-free and easy implementable nature at a specific rate and length is the prime focus point here. Current build methods were somehow restricting or compromising one or other factors of requirements. Based on good performance and hardware compliance, construction methods over a broad spectrum of frequencies and longitudes need to be developed.

The development and implementation of the LDPC hardware code depend on the LDPC layout target and are as diverse as the LDPC archives. The variables used in this algorithm: decoding estimates, network interconnection points, number of nodes, memory dimensions, numbers of bits of quantization and decoding delay. Day-to-day communications such as cloud networks, television broadcasting/weather digital satellite forecasting, internet, high-speed modems, wireless mobile phones are instances of automated communication systems symbolizing the transfer of information from the source to the insecure environment, namely space/air. These environments are unstable, and errors can occur during transmission. The original information is encoded to increase error correction capability.

2. Literature Review

The work [1], through NRI, the information is encoded at the transmitter module, which is determined precisely by human-based channel communication. The FPGA improves the existing signals at the receiver module. [2] describes the LDPC encoding techniques through an approximate lower triangulation model. By solving the triangular factorization and sparse equation, this technique computes the parity check symbols. [3] describes the LDPC decoder with less power. For calculating the count of iteration until the end of the LDPC decoding, the SNR evaluation value is utilized.

In [4], the encoding scheme method and soft-decision iterative decoding are described. In [5], the encoder in LDPC is substituted by the proposed encoding method by avoiding the transitions is described. This method offers less power. In [6], protograph LDPC codes over space-time block code over Rayleigh fading channels are described. Also, the comparison is made for bit error rates and decoding thresholds of two-protograph codes, namely accumulated-repeat-by-4-jagged-accumulate and accumulated-repeat-by-4-jagged-accumulate.

In [7], the architecture of hybrid coding is described. This coding is made up of optimized protograph LDPC and modified variable run-length limited codes to minimize the occurrence of error. In [8] low routing parallel decoder and iterative decoder convergence are described. To reduce the logic area and interconnect complexity is bit serial-parallel architecture is used. [9] describes the build of multiple rate LDPC codes, a modified progressive edge growth algorithm is too described. This technique is also named as multi-rate progressive edge growth, and this minimizes the realization complexity.

In [10], the hardware architecture of parallel decoding and encoding approach for polar codes concatenation with LDPC is described. This approach reduces the decoding delay. In [11], IEEE 802.16e based decoder is described. This method provides less latency. In [12], a variable length coding approach utilizing LDPC is described for lossy compression. This approach is made up of lossless compression module and vector quantization module.

In [13-15], optimization techniques for parallel LDPC decoder is described. It contains fully coalesced memory access, multi-stream concurrent kernel execution and asynchronous data transfer for new GPU structure is utilized. In conventional LDPC encoding and decoding, a parallel, parallel encoding and decoding Algorithm with reduced latency and power consumption is presented with long latency and high power to overcome these disadvantages.

3. Method

3.1 LDPC Code Detection

General-purpose microprocessors are employed with a high level of flexibility concerning reconfiguration and quick deployment characteristics in the SDR deployment and prototyping phase. Multipurpose Microprocessors, on the other hand, are not specialized in complex calculations and maybe power inefficient. Digital signal processors (DSP), which are specialized in

digital computing, are relatively simple to implement new digital communication modules. The processor is relatively power-efficient. DSPs, however, are not appropriate for rigorous computational procedures and can be lent. Field Gate Arrays are essential for custom digital signal processing applications since specialized algorithms can be implemented that are entirely parallel. The DSP framework facilitates the creation of new modules and FPGAs. MATLAB functions are used to generate the corresponding Verilog and VHDL codes for implementation purposes too. Moreover, simulation models and state flow charts are also perfect for extracting signal processing algorithms from specific MSP slice programs. DSP applications use many of the binary multipliers and accumulators that we may use in dedicated DSP slices.

The proposed LDPC code detection system includes mapping some word or message information to a long-word code with a one-to-one connection for every word and its related text field. This correlation is required if the same knowledge is to be recovered from the word. Traditionally, the length of the word description is taken as K, while the size of the word code is N. Therefore, the coding process provides consistency,

$$M = N - K \tag{1}$$

Additional elements in any word code such as Binary codes are used in this analysis, indicating that every part of the message and code words is either *0* or *1*. Besides, the coding schemes used are assumed to be hierarchical, unless otherwise specified. The message word for systematic systems is found in the code word as in equation 1, 2 shown

$$c = [M\ p] \tag{2},$$

where p is the redundant bit length M is the message length vector of the encoder. This indicates the amount of redundancy that the code has introduced, thus

$$R = K/N = (N - M)/N \tag{3}.$$

LDPC codes are linear block codes, fully defined in the matrix of code known as the matrix of parity checks for the code. In the case of binaries, the C-code (N, K) is officially specified in the Galois binary field of all N-tuples as a K-sized subspace. For linear block code, the parity-check matrix is binary $M = N$ matrix H so that C is zero-space H. You may also define the linear block code as a binary K / N generator matrix G, a matrix with a row space equal to C. It is clear from these definitions that for every $C \in C$

$$c = mG \tag{4}$$

$$cHT = 0 \tag{5}$$

where the two operations are performed under arithmetic modulo-2, LDPC codes are linear block codes with a sparse parity check matrix, as seen in Equations (4), and (5). The LDPC matrix H has a higher non-zero compared with zero inputs. LDPC codes have a higher parity check matrix.

3.2 LDPC Representation

Although a sparse matrix determines an LDPC code, Tanner graph, a two-part graph, can be used to represent the code. A Tanner two-part graph is a graph with nodes divided into two sets that connect each node to a node in the other set. The two nodes in a Tanner graph, known as check nodes and factor nodes, describe rows and columns. Figure 2 displays a matrix with a matching Tanner graph for the parity check. If and only if *H=a*, then *b = 1*. The check network a is equipped to the variable node Search Nodes *f0*, while *b* to *F5* reflect the matrix 's six rows, and columns *V0 …V11*.The same number of elements in each check node corresponds to the mass of the row. The number of edges in each reference node corresponds to the weight of the column. In this case, the weights are four and two in row and column, respectively. A loop for parity checking in a matrix is generated through a complete path through *1* input with alternating movements between rows and columns. The cycle length is a function of the number of edges moving in the direction. In the graph, a cycle of six is shown in bold. In a Tanner graph or matrix for parity search, the smallest cycle is called its girth. The least girth possible is four. A bipartite graph has a minimum length cycle of four and even cycle lengths.

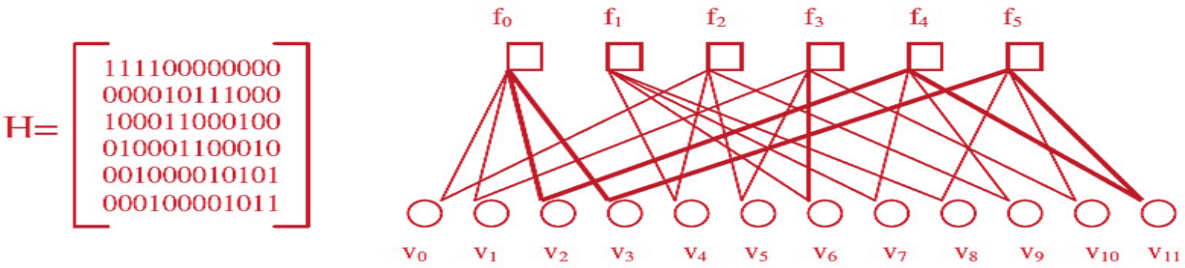

Figure 2: Parity test matrix

3.3 LDPC Encoding

The encoding process of LPDC code is achieved in the similar way for all linear systems using the LDPC representation technique briefly discussed above. For the given or known H matrix, the generator matrix *G* is derived from the values to check the parity errors. The encoded matrix 'c' is achieved by multiplying the generator matrix with *u = u1 … uN* such as *c = uG*, where *u* is a string of bits. Note that placing *H* in a systematic form, *H = [PT IM]*, would no longer have fixed column or row weights and most likely *P* would be dense. The computational complexity of the proposed encoder is calculated by the density of *P*. A complex generator matrix requires many complex computations when combining the pattern with the data to be sent. The complexity of the encoding process is the number of operations $O(N^2)$ or, more specifically, operations $N^2 R(1-R)$ where *R* is code rate. The preprocessing technique over the parity-check matrix can reduce the complexity of the encoding process for specific codes. An effective encoding technique was developed to minimize encoding difficulties to *O(N)* by rearranging the matrix for parity checks before encoding. The complexity of encoding also depends upon the code 's structure (row-column interconnections). Quasi-cyclical codes are one where another codeword results in a cyclic shift of

one codeword. Thanks to the cyclic row-column ties, due to this encoding process result as linear with the code length

3.4 LDPC decoding

Decoding process of LDPC code attempts to reconstruct the received codeword c probably from the corrupted word obtained, that is y. It's accomplished with the use of matrix parity search H. The condition that $cH^T = 0$ defines the collection of parity test constraints or equations to be met in order to obtain the codeword to be the same as the codeword to be passed. The matrix used for parity regulation constraints are

$$\begin{aligned} v0 + v1 + v2 + v3 &= f0 \\ v4 + v6 + v7 + v8 &= f1 \\ v0 + v4 + v5 + v9 &= f2 \\ v1 + v7 + v8 + v10 &= f3 \\ v2 + v7 + v9 + v11 &= f4 \\ v3 + v8 + v10 + v11 &= f5 \end{aligned} \quad (6).$$

If the values for the variable node-set is a valid code, then each constraint equation is equal to zero. The comparisons are generalizable using equation 7 in the form

$$fa = \bigoplus Hab = 1vb \quad (7),$$

$$a = 1 \ldots M, b = 1 \ldots N,$$

where fa is H's ath row, and vb the bth column, the equations for parity checks are constructed from each row of the matrix.

The LDPC structure is made up of random bits transmitted through the AWGN channel and finally, the output is attained through LDPC decoder. In the encoder module, by multiplying the message block with the generator matrix, the information bits are coded to achieve the code words. Figure 3 shows the optimized LDPC Encoder.

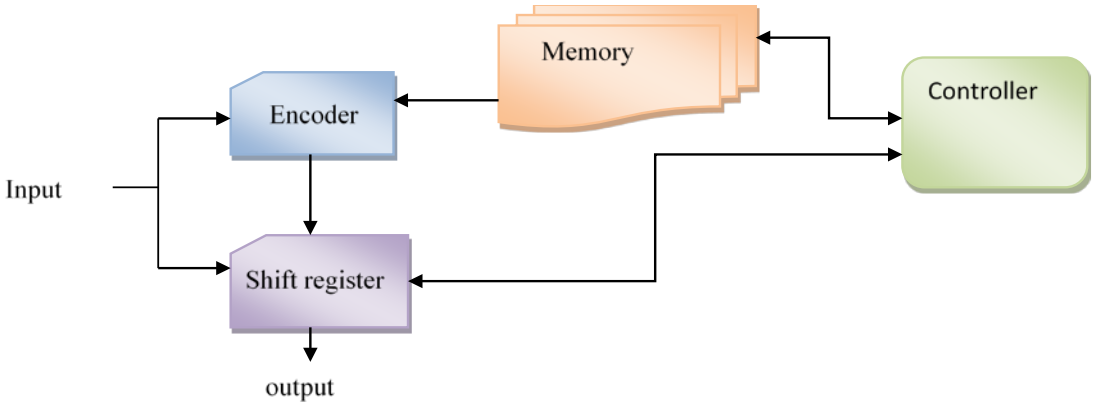

Figure 3: Optimized LDPC encoder blocks

The core of the encoder is the binary vector multiplication of the message which results in each parity bit, and there is one row of parity matrix. Memory, parity measurements, and codeword storage are used in the controllers for synchronization of message and parity check bits. In the decoder module, the parallel iterative structure is used with less hardware complexity. Figure 4 shows the optimized parallel LDPC decoder structure.

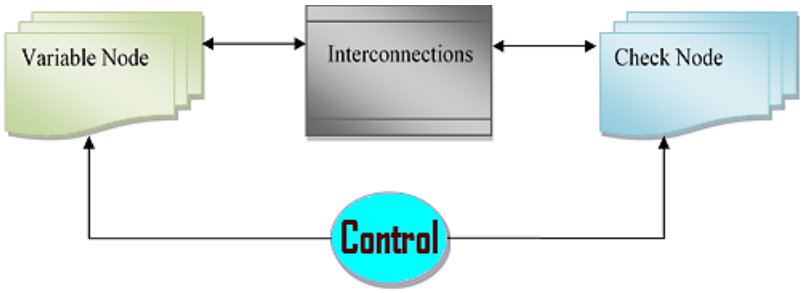

Figure 4: Optimized LDPC decoder blocks.

Optimized LDPC decoder has a separate variable and checks nodes with a highly parallel structure bypassing the message bit serial. To reduce the latency of the performance, the main consideration is the timing of the decoder by limiting the critical path through the nodes. Also, the power consumption for this design provides less dissipation.

4. Result and Discussion

The optimized LDPC encoder and decoding is designed using Xilinx 12.4 ISE tool and simulated using Verilog language. Figure 5 show the simulation result of the optimized LDPC encoder, representing the encoder waveform, the encoded output is low when the reset is low, and the message 01110101 is encoded as 010011100101. The output of the encoder will vary according to the messages.

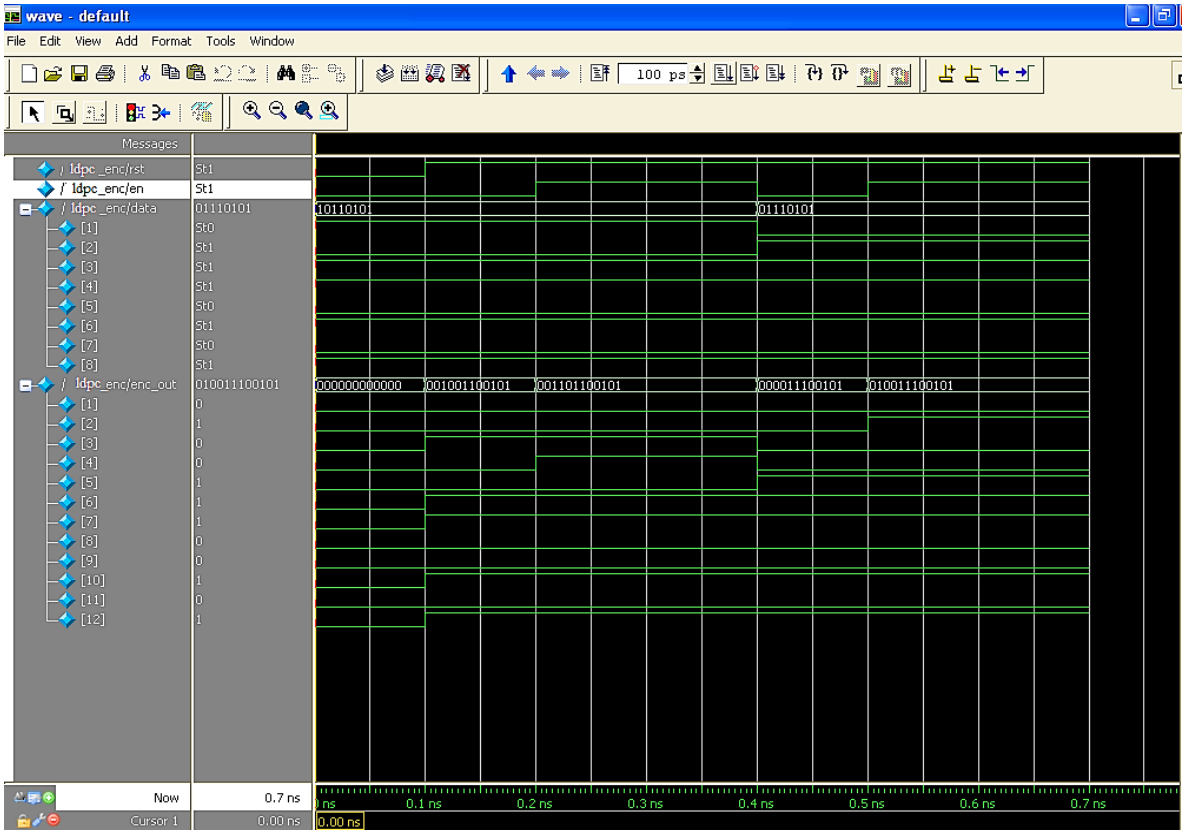

Figure 5: Simulation result of optimized LDPC encoder.

Figure 6 shows the simulation for the LDPC decoder, the decoder waveform. The decoded output is low when the reset is high, and when the resets are low, the received code is *01110101* is encoded as *010011100101*. The decoded output will vary according to the proposed technique used.

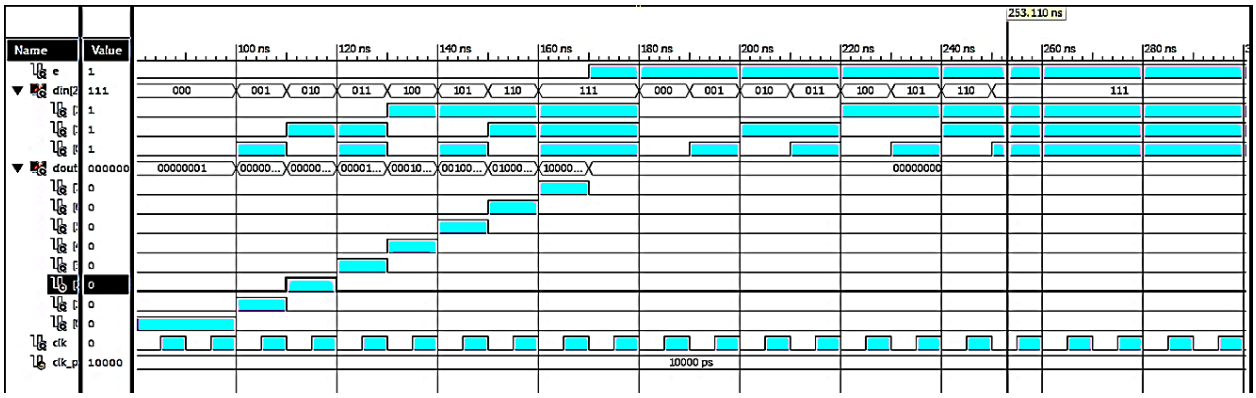

Figure 6: Simulation result of optimized LDPC decoder

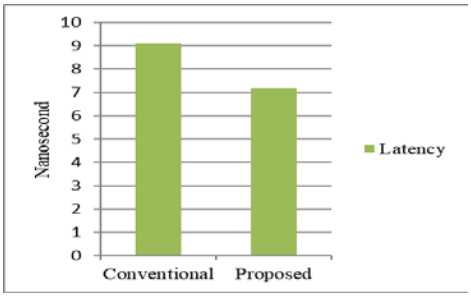

Figure 7: Performance comparison of Latency parameter.

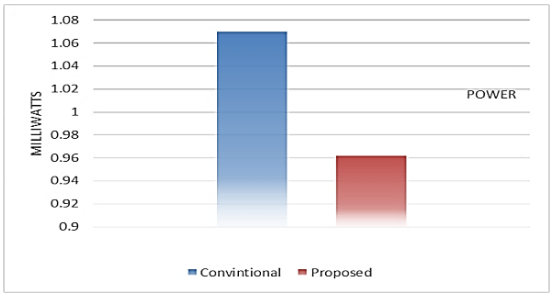

Figure 8: Performance comparison of Power consumption.

Figure 7 and 8 describes the performance of the proposed LDPC method over the conventional [1] LDPC encoder and decoder, where conventional method offers 9.1ns latency while the proposed design offers only 7.2*ns*. Similarly, the power consumption for the conventional design is 1.07 mw and for proposed design is 0.962 *mw*. This analysis proves the proposed design offers less latency and power consumption compared to the conventional design. This technique is an efficient tool for SDR communication.

5. Conclusion

The proposed system is developed and verified through obtained results using the Xilinx platform. This result is encouraging for SDR applications that require advanced-spectral characteristics with quality communication, along with improved decoding efficiency. This power-optimized algorithm is useful for the baseband encoding/ decoding processes at low cost, real-time radio receiver devices. The proposed LDPC encoder and decoder are designed and implemented in the Xilinx ISE platform. The main advantage of this iterative decoding process is low-power consumption. Generally, the LDPC is a good error-correcting code for the low-end applications in the past. This optimized parallel-structured LDPC encoder and decoder offers better performance in terms of 20.87 percent reduction in latency and 9.01 percent reduction in power consumption in comparison with the conventional method without degrading performance with less hardware complexity. This study can now be used in high-end wireless communication protocols too.

6. Availability of Data and Material

Data can be made available by contacting the corresponding author.

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