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Design and Memory Optimization of Hybrid M-GDI Numerical Controlled Oscillator

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Abstract

A numerically Controlled Oscillator (NCO) was a digital oscillator signal generator that forms synchronous, clocked, discrete waveforms, normally sine. Numerically Controlled Oscillators were frequently utilized in combination with DAC at the outcome to generate a Direct Digital Synthesizer (DDS). A numerically Controlled Oscillator was utilized in several communications devices that were absolutely digital or assorted-signal, such as arbitrary waveform synthesis, the precise regulator at phase array radar systems, most digital Phase-Locked Loop, Digital Down/Up converters for Cellular and base stations and drivers for optical or acoustic transmissions and multi-level Frequency Shift Keying/ Phase Shift Keying modulators or demodulators (modem). In this analysis, the design and memory optimization of a hybrid Modified Gate Diffusion Input (M-GDI) numerically controlled oscillator is implemented. From the results, it can observe that compared with NCO-based 8-bit Microchip and Memory optimization of hybrid Gate Diffusion Input (GDI) NCO, Memory optimization of hybrid M-GDI NCO gives effective outcomes in terms of delay, MOSFET's and Nodes.

Discipline: Communication Engineering.

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1 Introduction

Several Digital Signal Processing (DSP) systems need the formation of sine waves/different periodic waveforms. A technique for forming the signals requires "Numerically Controlled Oscillators" in digital accumulators was utilized to form the address into a sine LUT. (Different operations save in the LUT, generating "arbitrary waveform generator"). This device was highly normal in hardware as well as in software [1]. That enables immediate modifications in the immediate frequency or phase of the formed waveform, during sustaining an uninterrupted phase property as result. If integrated with a DAC to generate an analog outcome waveform, the system was known as DDS.

NCO was a digital signal generator that forms synchronous (clocked), discrete-time, and value presentation of the waveform, normally sine. Numerically Controlled Oscillators were frequently utilized in

conjunction with a DAC result to form DDS. NOCs produce many benefits from different kinds of oscillators are agility, accuracy, stability, and reliability. Numerically Controlled Oscillators were utilized in several communications devices involving digital up/down converters utilized in 3G wireless and software radio systems, digital Phase-Locked Loops, radar systems, drivers for optical or acoustic transmission, and multiphase Frequency Shift Keying/Phase Shift Keying modulators or demodulators [2-4]. NCO was an electronic device for the synthesis of a range of frequencies of a decisive time base. Dissimilar PLL-based analog frequency synthesizes are efficient in synthesizing the most extensive precise frequency ratio range.

NCOs known as DDS was a strong method utilized by radio frequency signals formation operation in different approaches from radio receivers to signal generators and so on. A standard NCO utilizes a time domain amplitude sample to form a sine wave as the range was regulated by digital control words in the phase of a single clock cycle [5]. A Numerically Controlled Oscillator resultant frequency may modify immediately in the absence of accession and lock time delays combined with standard Phase Locked Loop (PLL) synthesizers. The Numerically Controlled Oscillators result frequency was regulated by an input count/integer value [6-14].

The inner design of a Numerically Controlled Oscillator core normally contains a phase accumulator as well as Phase-to-Amplitude Converter (PAC). All PACs utilize 2 or many LUT and few combined logic produce PACs. For saw-tooth wave generation that utilizes the logic of a counter and for the formation of Sine / Cosine wave that uses Rom (that saves the outputs of Sine and Cos) [15]. Based on the input counts if sent to this block, they will choose the numbers from the Read Only Memory that in turn was the Sin / Cos wave. In this analysis, they did the coding for here and explained the logic to form a saw tooth and a sine wave.

2 NCO Overview and Derivation

A numerically Controlled Oscillator will utilize to form a large kind of regular result waveform, and for the reason of record, cos result operation is guessed.

$$y[n] = \cos(\varphi[n]) \quad (1).$$

In this part, argument φ[n] was the immediate level for the resulting signal of nth outcome sampling [16-18]. As a sample, the stable outcome frequency for f0 cycles per cycle, and stable outcome level θ0 radius,

$$\varphi[n] = 2\pi f0n + \theta0 \text{ giving } y[n] = \cos(2\pi f0n + \theta0) \quad (2).$$

Anyhow, else frequency and phases were modified by ‘n’, instantaneous frequency fi [n] gives enhancement to φ[n] that might be collected before the period, and during instantaneous phase offset θi [n] gives an offset outcome was implemented alone with nth test [19].

$$\varphi1[n] = \varphi1[n-1] + 2\pi fi\,[n],\ \varphi[n] = \varphi1[n] + \theta i\,[n] \quad (3)$$

A Numerically Controlled Oscillator contains 2 basic blocks: a digital “phase accumulator” that executes an evaluation of (2), and a “phase-to-amplitude converter” [20-22] that changes outcomes φ(n) to form the result example numbers provided by (1). The numerically Controlled Oscillator framework is explained in Figure 1.

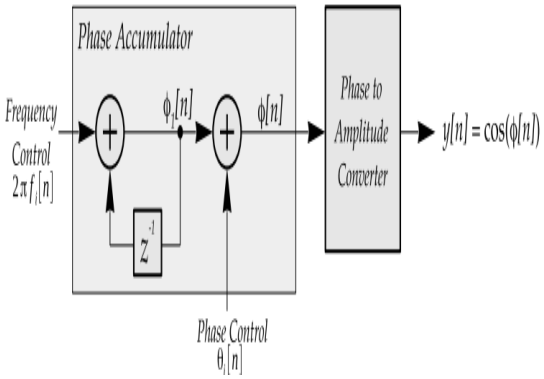

Figure 1: Numerically Controlled Oscillator Conceptual Structure.

2.1 Phase-To-Amplitude Converter

The capability of PAC generally contains a table for saved pre-evaluated outputs for cos() operation of phase outcomes enclosing one rotation. The input of φ[n] was obtained modulo-2π and circled to notice the nearby approach in table [23]. Index evaluation into the table was mostly easier when table length N was chosen with the integer power of 2: N = 2m. Here, the modulo function forming address into saved table includes easier choosing the accurate m bits of phase presentation. Suppose the outcomes saved in Table 1 were provided by

$$yk = \cos(2\pi k/N),\ k = 0, 1, 2. \ldots, N - 1\ (N = 2m) \quad (4).$$

Provided the required cos argument of φ[n], table index was acquired by keeping φ[n] = 2πk/N and resolving [24]:

$$k = N/2\pi\ \varphi[n] \quad (5).$$

The output index was circled as well as provided modulo N. Equation (3) is unutilized[25-28]. Rather, equation (2) was calculated by the value of N/2π hence phase accumulation straightly produced the needed tabular index.

2.2 Phase Accumulator

The phase accumulator executes evaluation of (2), calculated by value N/2π thus, an accurate index in LUT was formed straightly. Let k1[n] and k[n] denotes the index that combines φ1[n] and φ[n]. Calculating (2) with N/2π provides needed addresses evaluation [29-30]:

$$k1[n] = k1[n - 1] + Nfi\ [n],\ k[n] = k1[n] + N\ /2\pi\ \theta i\ [n] \quad (6).$$

The accumulator developed the integer register which enables the "wrap", hence modulo function needs without excessive hardware or rules [31]. Phase accumulator accuracy can enhance by executing evaluation in the register that was greater than m bits, as well as later utilizing great-important m bits output for the formation of index into LUT. Predict M > m bits were utilized. (As a sample, M = 32 will be a normal alternative for design having 32-bit registers.) Verified accumulator evaluation was acquired by calculating (4) by the value of 2M−m. Explain k 0 [n] = 2M−mk[n] and k 0 1 [n] = 2M−mk1[n] as constantly formed at the M-bit register [32]. Calculating (4) by 2M−m, as well as recording the 2M−mN = 2(M−m)2 m = 2M provides M-bit register evaluation:

$$k1\ [n] = k\ 0\ 1\ [n - 1] + 2^{M}fi\ [n],\ k0\ [n] = k\ 0\ 1\ [n] + 2^{M}/\ 2\pi\ \theta i\ [n] \quad (7).$$

An outcome of k[n] was acquired by a great important m bit of k 0 [n]. The output was utilized to index into LUT. The output of enhanced word size for phase accumulator, the frequency can identify accuracy with a single portion of 2M [33-34].

Depending on the input frequency, the Numerically Controlled Oscillators phase accumulator provides an output that addresses a sine-cosine lookup table [35-38]. The Sin/Cosin Lookup block provides the actual difficult sinusoidal signal.

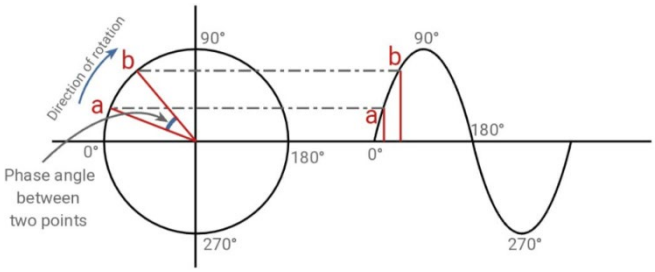

Figure 2: Phasor Diagram of NCO.

NCO was largely utilized in the generation of sinusoidal waveforms in DSP. An NCO is a system that provides a digital approximation to a sin or cos wave related to a modification in its input. The standard application to develop these oscillators is to use Look Up Tables (LUT) for forming the waveforms [39]. That developed a Numerically Controlled Oscillator by the similar p as explained in section 2 above as an input. Here, the needed frequency (f) of sin or cos signals was produced based on the input beta p that was presented as 8-bit 2's complement as shown in Figure 2 [40].

3 Literature Survey

3.1 An Improved Analog Waveforms Generation Technique using a Direct Digital Synthesizer

In several types of apparatus, it was significant to provide quick control and appropriate waveforms in different frequencies and profiles like agile frequency sources with low phase noise and low spurious signal content for communications, as well as easily formed frequency for industries and biomedical approaches [41]. DDS produces more important benefits by the Phase-Locked Loop performances like Continuous-phase switching response; fine frequency resolution, Fast settling time, and low phase noise are parameters simply available in Direct Digital Synthesizer systems. This analysis goal begins with the Direct Digital Synthesizer device framework and explains the Direct Digital Synthesizer model technique depending on VHDL in particular [42-45].

3.2 Realization of FPGA Based Numerically Controlled Oscillator

NCO was a significant element in several Digital Communication Systems like Digital Radio and Modems, Software Defined Radios, Digital Down/Up converters for Cellular and PCS base stations, etc. The general method for the digital generation of difficult or real-valued sinusoidal works as a LUT-based plan. Simulation and optimization of the Numerically Controlled Oscillator model were initially utilized software tool Xilinx 10.1 and later coded in VHDL for Hardware Realization. These models were examined on the Xilinx Spartan2 FPGA Development Platform. Examined outputs were similar to particular and simulated outputs. This analysis explains an FPGA-based development technique that could highly enhance the execution, shorten the development cycle, and decreases cost.

3.3 Design and Implementation of a Feasible Direct Digital Synthesizer to Eliminate Manual Tweaking

This analysis explains designs and simulations of the programming model of the greatest and accessible DDS which avoids the requirement for non-automatic tuning and tweaking relevant to element condition and temperature drift in analog synthesizer solution. A DDS computed portion o DDC the DDC (Digital Down Converter) had turned into a cornerstone method in communication systems. DDC was an important element for RF systems in communications, sensing, and imaging. The analysis calculates the execution of the Digital Down converter by different programming aspects and ultimately executes the realization of the Digital Down Converter utilizing Virtex II Pro.

3.4 An FPGA-based Spur Reduced Numerically Controlled Oscillator

DDS or NCO are significant elements in several digital communication systems, like digital radios and modems, software-defined radios, digital down/up converters for cellular and PCS base stations, etc. The general technique for digital forming difficult/real-valued sine works as a LUT scheme. This analysis provides an FPGA-based technique that could important decrease the Spurious Free Dynamic Range (SFDR). A suggested model was developed on Xilinx Virtex 5 FPGA and simulated outputs were considered by earlier outputs to describe important improvements in decreasing SFDR.

3.5 The Design of Digital Down Converter Based on FPGA

The primary concept of DDC in the digital receiver is explained in this analysis. Xilinx ISE 13.3 software is selected to sketch every module of DDC. Later utilizes Modelsim 6.5 simulated operation to check functionality exactness of design. The simulation result signals were examined in the outputs in Matlab.

4 Modified GDI NCO

One of the most important parts of digital down conversion is NCO. The NCO is most widely utilized in software radio systems as well as in radar wireless transceiver systems. Here the NCO major function is producing two path sine and cosine data samples with discrete time, variable frequency and mutually orthogonal. The main advantage of NCO is quick response and high-frequency precision. The LUT and polynomial expansion are the traditional implementation methods of NCO. The LUT method data accuracy depends on the LUT size of ROM. The memory size and phase accuracy precision are the exponential relationships that will enlarge the consumption of resources and reduce the system processing speed.

As known that NCO is one of the most utilized digital oscillators that generate signals like clocked, discrete and synchronous waveforms. The NCOs are more often utilized in combinations with the DAC at the outputs for creating DDS. The NCO is utilized in various communication systems that are fully digital or mixed signals such as synthesis of the arbitrary waveform, phased array radar and precise control.

Figure 3 shows the schematic of **the** Memory optimization of hybrid GDI NCO. In this 16 MOSFET's are utilized to design. 2 MOSFET's geometries are utilized. Basically, total nodes are classified into two types boundary nodes and independent nodes. 1.70 seconds is taken to execute the entire second. 0.14 seconds is taken for parsing and 0.03 seconds is taken for setup of the design. 12 total nodes are utilized, and 5 boundary nodes and 7 independent nodes are utilized. Compared with NCO-based 8-bit microchip design, memory optimization of hybrid GDI-based NCO gives effective outcomes in terms of delay, MOSFET's and nodes.

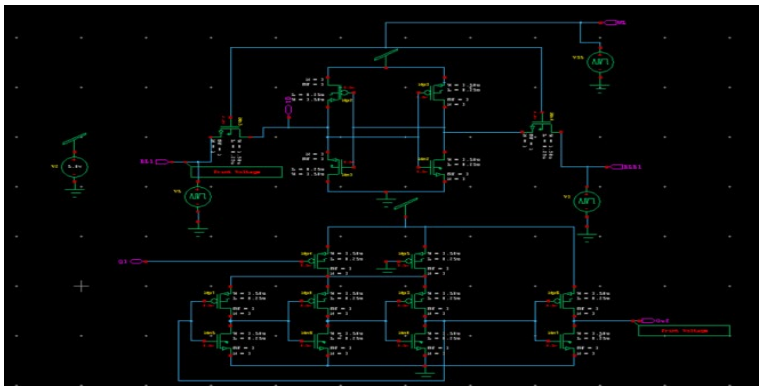

Figure 3: Schematic Design.

5 Results and Discussion

Table 1 shows the comparison table. In this NCO-based 8-bit Microchip, the Memory optimization of hybrid GDI NCO and Memory optimization of hybrid M GDI NCO parameters are given in a detail manner.

Table 1: Comparison Table.

S.No	Parameters	NCO Based 8 bit Micro chip	Memory Optimization of Hybrid GDI NCO	Memory Optimization of Hybrid M GDI NCO
1	MOSFET'S	32	16	11
2	MOSFET'S Geometries	5	2	1
3	Voltage Sources	8	4	2
4	Total Nodes	26	12	9
5	Boundary Nodes	14	5	4
6	Independent Nodes	12	7	5
7	Total Delay	2.51 Seconds	1.70 Seconds	1.40 Seconds
8	Parsing Delay	0.43 Seconds	0.14 Seconds	0.11 Seconds
9	Setup Delay	0.06 Seconds	0.03 Seconds	0.02 Seconds
10	Overhead Delay	0.81 Seconds	0.78 Seconds	0.74 Seconds
11	DC Operating Point	0.74 Seconds	0.70 Seconds	0.67 Seconds
12	Transient Analysis	0.06 Seconds	0.04 Seconds	0.02 Seconds

Figure 4 shows the comparison of nodes for an NCO-based 8-bit Microchip, Memory optimization of hybrid GDI NCO and Memory optimization of hybrid M GDI NCO. Compared with NCO-based 8-bit Microchip and Memory optimization of hybrid GDI NCO, Memory optimization of hybrid M GDI NCO uses less number of nodes.

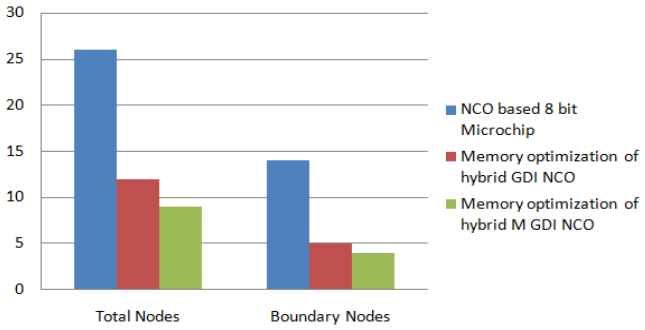

Figure 4: Comparison of Nodes.

Figure 5 shows the comparison of delay for NCO-based 8-bit Microchip, Memory optimization of hybrid GDI NCO and Memory optimization of hybrid M GDI NCO. Compared with NCO-based 8-bit Microchip and Memory optimization of hybrid GDI NCO, Memory optimization of hybrid M GDI NCO produces less delay.

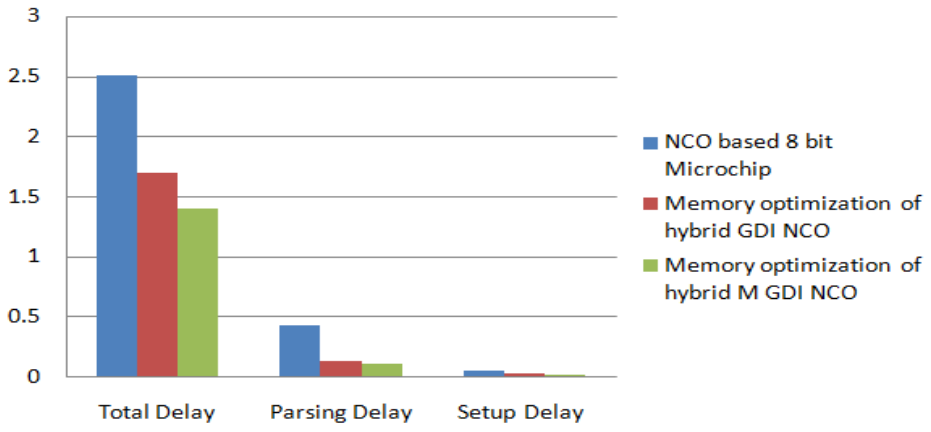

Figure 5: Comparison of Delay.

Figure 6 shows the comparison of NCO-based 8-bit Microchip, Memory optimization of hybrid GDI NCO and Memory optimization of hybrid M GDI NCO. Compared with NCO-based 8-bit Microchip and Memory optimization of hybrid GDI NCO, Memory optimization of hybrid M GDI NCO uses fewer MOSFET's.

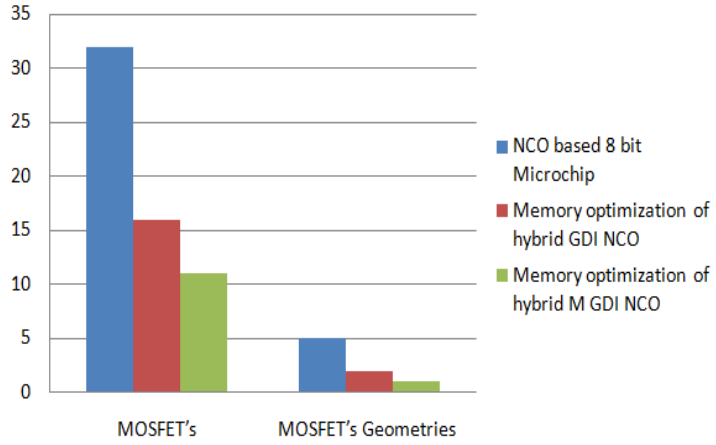

Figure 6: Comparison of MOSFET'S.

Figure 7 shows the comparison of transient analysis, overhead delay, and DC operating point for NCO-based 8-bit Microchip, Memory optimization of hybrid GDI NCO and Memory optimization of hybrid M GDI NCO. Compared with NCO-based 8-bit Microchip and Memory optimization of hybrid GDI NCO, Memory optimization of hybrid M GDI NCO takes less time.

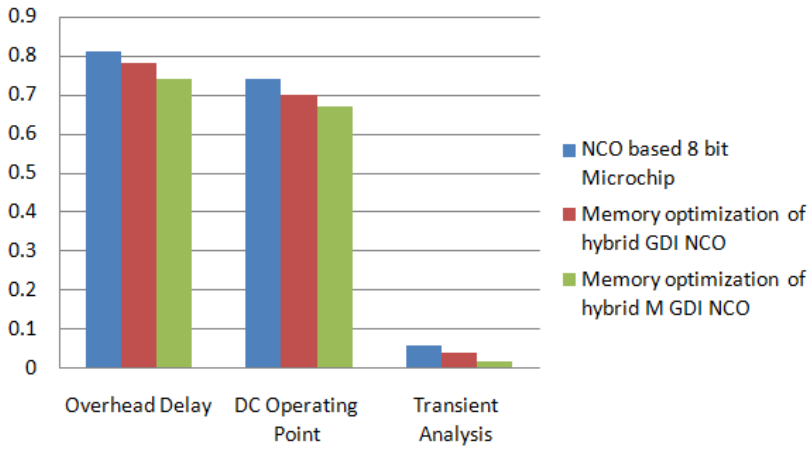

Figure 7: Comparison of Transient Analysis, Overhead Delay and DC Operating Point.

6 Conclusion

Hence in this paper design and memory optimization of a hybrid M-GDI numerically controlled oscillator was implemented. The NCO is an electronic architecture to incorporate the scope of frequencies from changing time bases. Unlike a simple recurrence synthesizer based on stage bolted circles, the NCO fits to combine the extensive varieties of exact recurrence proportions. In addition, the NCOs known as DDS is an intensive method utilized as a part of the radio recurrence signals era to apply in utilizations assortment from radio collectors for signs generators and certainly more. From the results, it can observe that compared with NCO-based 8-bit Microchip and Memory optimization of hybrid GDI NCO, Memory optimization of hybrid M GDI NCO gives effective outcomes in terms of delay, MOSFET's and Nodes.

7 Availability of Data and Material

Data can be made available by contacting the corresponding authors.

8 References

[1] Siva Subramaniyam C N; Deepa Venkitesh, "Experimental Demonstration Of Multimode Optoelectronic Oscillator At 2.4 Ghz", 2022 Workshop On Recent Advances In Photonics (Wrap).

[2] Yichao Yuan; Chung-Tse Michael Wu, "Recent Development of Super-Regenerative Oscillator (SRO)-Based Vital Sign Radar Sensors", 2022 IEEE MTT-S International Microwave Bio Conference ((IMBIOC).

[3] Hao-En Liu; Wei-Cheng Chen; Hong-Yeh Chang, "A W-band Quadrature Voltage-Controlled Oscillator with an Injection-Locked Frequency Divider in 40-nm CMOS Process", 2021 IEEE International Workshop on Radio-Frequency Integration Technology (RFIT).

[4] Hao Zhou, "A K-band Differential-output GaAs pHEMT Voltage Controlled Oscillator", 2021 International Conference on Integrated Circuits and Microsystems (ICICM).

[5] Soyeon Choi; Yerin Shin; Hoyoung Yoo, **"**Analysis of Ring-Oscillator-based True Random Number Generator on FPGAs", 2021 International Conference on Electronics, Information and Communications (ICEIC).

[6] S. Roy, "Cordic algorithm and its implementation," Jan 2019. [Online]. Available: https: //digitalsystemdesign.in/wpcontent/uploads/2019/01/cordic1.pdf

[7] N. Pang, H. Q. Mu and P. J. Xu, Wide-band digital down conversion technique based on poly-phase ¯lter, International Radar Conference IET (Hangzhou, 2015), pp. 1–5.

[8] Priyankap. Chopda, Kavita S. Tated&Jayant J. Chopade, "Sine Wave Generation Using Numerically Controlled Oscillator Module", BEST: International Journal of Management, Information Technology and Engineering (BEST: IJMITE) ISSN(P): 2348-0513;ISSN(E): 2454- 471X Vol. 3, Issue 7, Jul 2015, 35-40.

[9] Gopal D. Ghiwala, Pinakin P. Thaker, GireejaD.Amin, "Realization of FPGA based numerically Controlled Oscillator", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 5, PP 07-11, (Jan. - Feb 2013).

[10] T. Liu, S. L. Tian, Z. G. Wang and L. P. Guo, An efficient parallel architecture for wideband digital down conversion, J. Comp. Info. Syst. 18 (2013) 7315–7324

[11] P. C. Pedersen, "Digital generation of coherent sweep signals," IEEE Transactions on Instrumentation and Measurement, vol. 39, issue 1, pp. 90-95, February 2013

[12] Gopal D. Ghiwala, Pinakin P. Thaker, GireejaD.Amin, "Realization of FPGA based numerically Controlled Oscillator", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 5, PP 07-11, (Jan. - Feb 2013).

[13] Gaurav Gupta, Monika Kapoor, "An Improved Analog Waveforms Generation Technique using Direct Digital Synthesizer", International Journal of Computer Applications (0975 – 8887) Volume 78 – No.5, September 2013.

[14] Gopal D. Ghiwala, Pinakin P. Thaker, GireejaD.Amin, "Realization of FPGA based numerically Controlled Oscillator", IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 5, PP 07- 11, (Jan. - Feb 2013).

[15] SnehalGaikwad, KunalDekate, “Design and Implementation of Feasible Direct Digital Synthesizer to Eliminate Manual Tweaking”, IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 2, Issue 4, , PP 53-56e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197,(May. – Jun. 2013).
[16] Guoping Wang, Dalian,“An FPGA-based SpurReduced Numerically Controlled Oscillator”, International Conference on System Science and Engineering,p.p 187-192 2012.
[17] Guoping Wang, Dalian,“An FPGA-based SpurReduced Numerically Controlled Oscillator”, International Conference on System Science and Engineering,p.p 187-192 2012
[18] M.Saber, Y.jitsumatsu & M.T.A.khan,“A Simple Design to Mitigate Problems of Conventional Digital phase locked loop”,An international journal(SPIJ),vol 6,issue 2,p.p 65-77,2012
[19] JunmingYe,GuangxiangZhou, Haiyan Liu,“Design and Research of Improved Digital Phase-Locked Loop Based on FPGA”, International Workshop on Information and Electronics Engineering,Procedia Engineering 29 p.p547 – 552,2012.
[20] Q. X. Zhang and X. X. Su, The design of digital down converter based on FPGA, IEEE. Int. Congr. Wirless Communications, Networking and Mobile Computing (Shanghai, 2012), pp. 1–4.
[21] Shuhua Hu, Hui Li, Jiaqing Huang ,“An Optimal Algorithm for Designing NCO Circuit In Mobile Communication Systems”,International Conference on Communications and Mobile Computing, p.p 372- 376,2009.
[22] Sameer Kadam, Dhinesh Susidaran, Amjud Awuwdeh,LouisJohnson,MichaelSoderstrand, “Comparision of various Numerically Controlled Oscillators” Oklahoma state university,p.p 200-203,2002.
[23] Shuhua Hu, Hui Li, Jiaqing Huang ,“An Optimal Algorithm for Designing NCO Circuit In Mobile Communication Systems”, International Conference on Communications and Mobile Computing, p.p 372- 376,2009.
[24] Sameer Kadam, Dhinesh Susidaran, Amjud Awuwdeh,LouisJohnson,MichaelSoderstrand, “Comparision of various Numerically Controlled Oscillators” Oklahoma state university,p.p 200-203,2002.
[25] ShubhadaDeo,SreerajMenon,Saritha Nallathambhi and Michael A. Sodershand.“Improved Numerically Controlled Digital Sinusoidal Oscillator”,IEEE, p.p 211-214,2002.
[26] Grezegorzpopek, mariankampik "Low-spur Numerically controlled approximation" Silesian university of technology, p.p 30-33, 2009.
[27] Sung, T.-Y., Hsin, H.-C, “Design and simulation of reusable IP CORDIC core for special-purpose processors”,Computers & Digital Techniques, IET Volume: 1 Issue: 5,Sept. 2007 Page(s): 581-589.
[28] IreneuszJaniszewski, Bernhard Hoppe, Associate Member, IEEE, and Hermann Meuth, “Numerically Controlled Oscillators with Hybrid Function Generators”, IEEE transactions on ultrasonics, ferroelectrics, and frequency control, vol. 49, no. 7, july.
[29] Hans-JorgPfleiderer, Stefan Lachowicz, “Numerically controlled oscillators using linear approximation”, 978- 1-4244-3892-1 /09/$25.00 ©2009 IEEE
[30] IreneuszJaniszewski, tBemhard Hoppe, and Hermann Meuth, FH Darmstadt, Darmstadt, Germany, “Precision and performance of numerically controlled oscillators with hybrid function generators”, 2001 lEEE International Frequency Control Symposium and FDA Exhibition.
[31] Gopal D. Ghiwala, Pinakin P. Thaker, GireejaD.Amin, “Realization of FPGA based numerically Controlled Oscillator”, IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) ISSN: 2319 – 4200, ISBN No. : 2319 – 4197 Volume 1, Issue 5 (Jan. - Feb 2013), PP 07- 11.
[32] SnehalGaikwad, KunalDekate, “Design and Implementation of Feasible Direct Digital Synthesizer to Eliminate Manual Tweaking”, IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 2, Issue 4 (May. – Jun. 2013), PP 53-56e-ISSN: 2319 – 4200, pISSN No. : 2319 – 4197.
[33] Shachi P, R. Mishra, J. Ravi Kumar, “Counter Based Numerically Controlled Oscillator – A New Architecture” International Journal of Advanced Trends in Computer Science and Engineering, Vol.2 , No.1, Pages : 98-102 (2013) Special Issue of ICACSE 2013 - Held on 7-8 January, 2013.
[34] Priyankap. Chopda, Kavita S. Tated&Jayant J. Chopade, “Sine Wave Generation Using Numerically Controlled Oscillator Module”,BEST: International Journal of Management, Information Technology and Engineering (BEST: IJMITE) ISSN(P): 2348- 0513;ISSN(E):2454-471X Vol. 3, Issue

7 , 35-40, Jul 2015
[35] Manoj Kollam, S.A.S.KrishnaChaithanya, Nagarajukommu, "Design and Implemation of An Enhanced Dds Based Digital Modulator for Multiple Modulation Schemes", International Journal of Smart Sensors and Ad Hoc Networks (IJSSAN) Volume-1, Issue-1, 2011.
[36] SiamakMortezapour,Edward K. F. Lee, "Design of LowPower ROM-Less Direct Digital Frequency Synthesizer Using Nonlinear Digital-to-Analog Converter", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 10, OCTOBER 1999.
[37] SiamakMortezapour,Edward K. F. Lee, "Design of LowPower ROM-Less Direct Digital Frequency Synthesizer Using Nonlinear Digital-to-Analog Converter", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 34, NO. 10, OCTOBER 1999.
[38] PetterKällström, "Direct Digital Frequency Synthesis in Field-Programmable Gate Arrays", Institutionenförsystemteknik Department of Electrical Engineering, pp 6-13.
[39] Eva Murphy, Colm Slattery, "All about Direct Digital Synthesis", Analog Dialogue 38-08, August (2004), Available at: http://www.analog.com/analogdialogue.
[40] Gaurav Gupta, Monika Kapoor, "An Improved Analog Waveforms Generation Technique using Direct Digital Synthesizer", International Journal of Computer Applications (0975 – 8887) Volume 78 – No.5, September 2013.
[41] Menakadevi T. and Madheswaran M., "Design And Analysis Of Hybrid Wave Pipelined Phase Accumulator For Direct Digital Synthesizer", ARPN Journal of Engineering and Applied Sciences VOL. 6, NO. 11, NOVEMBER 2011, pp 52-61.
[42] Monika kushwaha, U. M Gokhale, "Design and Simulation of Direct Digital Synthesizer for Wireless Applications", Journal of The International Association of Advanced Technology and Science, Vol. 16 March 2015.
[43] Henry T. Nicholas, III, Henry Samueli, Bruce Kim, "The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects," Proc. 42nd Annual Frequency Control Symposium, June 1988, pp. 357- 363.
[44] R. Ertl and J. Baier, "Increasing the Frequency Resolution of NCO-Systems Using a Circuit Based on a Digital Adder," IEEE Trans. Circuits Systems II: Analog and Digital Signal Processing, vol. 43, Mar. 1996, pp. 266-269.
[45] Paul O'Leary and Franco Maloberti, "A Direct-Digital Synthesizer with Improved Spectral Performance," IEEE Trans. Communications, vol. 39, no. 7, July 1991, pp. 1046-1048.

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